Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (currently amended) A method for exposing at least two semiconductor wafers in an exposure tool, the method which comprises:

providing a first semiconductor wafer to the exposure tool for exposing the first semiconductor wafer;

aligning the first semiconductor wafer using determined values of a first set of alignment parameters that depend on characteristics of the two semiconductor wafers;

exposing the first semiconductor wafer with a first pattern using a combination of the first set of alignment parameters and a second set of alignment parameters that account for an exposure tool-offset;

calculating values of a set of parameters representing an overlay accuracy of the first pattern on the first semiconductor wafer using a formula for each of the ~~alignment~~ parameters of the set representing the overlay accuracy, the

formula being a function of each of the alignment parameters of the first set;

adjusting values of the second set of alignment parameters to correct for an overlay inaccuracy of the first pattern; and

aligning the second semiconductor wafer in response to the values of the second set of alignment parameters that have been adjusted and exposing the second semiconductor wafer.

2. (original) The method according to claim 1, which comprises:

providing the formula as a linear function of each one of the alignment parameters of the first set; and

providing each one of the alignment parameters of the first set with a coefficient that depends on the exposure tool that is used.

3. (original) The method according to claim 2, which comprises:

constructing a neural network for adjusting the formula for calculating the values of the set of parameters representing the overlay accuracy; and

comparing the values of the set of parameters representing the overlay accuracy with measured values for the set of parameters representing the overlay accuracy obtained in the inspection tool.

4. (original) The method according to claim 1, which comprises:

issuing a warning signal when one of the parameters of the set of parameters representing the overlay accuracy of the pattern increases beyond a predetermined tolerance level;

stopping processing with the exposure tool for conducting system maintenance in response to the warning signal; and

continuing with processing after resetting the exposure tool.

5. (original) The method according to claim 1, which comprises:

issuing a warning signal, when one of the parameters of the set of parameters representing the overlay accuracy of the pattern increases beyond a predetermined tolerance level; and

deriving the set of parameters representing the overlay accuracy of the pattern on the semiconductor wafer for a second time by measuring parameters with an overlay inspection tool after the first semiconductor wafer has been exposed with the pattern.

6. (original) The method according to claim 1, which comprises processing each semiconductor wafer in a next manufacturing step after being exposured without being inspected in an overlay inspection tool.

7. (original) The method according to claim 1, which comprises performing the step of adjusting the values of the second set of alignment parameters by calculating the values of the second set of alignment parameters from the values of the set of parameters representing the overlay accuracy using a formula that is a linear function having a respective coefficient for each of the alignment parameters of the second set of alignment parameters.

8. (currently amended) A method for exposing at least one semiconductor wafer in an exposure tool, the method which comprises:

providing the semiconductor wafer to the exposure tool for exposing the semiconductor wafer;

aligning the semiconductor wafer using determined values of a first set of alignment parameters that depend on characteristics of the ~~two~~ semiconductor ~~wafers~~ wafer;

calculating values of a set of parameters representing an overlay accuracy of a pattern on the ~~first~~ semiconductor wafer using a formula for each of the alignment parameters of the set representing the overlay accuracy, the formula being a function of each of the alignment parameters of the first set;

adjusting values of a second set of alignment parameters that account for an exposure tool-offset in order to correct for an overlay inaccuracy of the pattern; and

aligning the semiconductor wafer in response to the adjusting step using a combination of the first set of alignment parameters and the second set of alignment parameters, and exposing the ~~second~~ semiconductor wafer.

9. (original) The method according to claim 8, which comprises:

providing the formula as a linear function of each one of the alignment parameters of the first set; and

providing each one of the alignment parameters of the first set with a coefficient that depends on the exposure tool that is used.

10. (original) The method according to claim 9, which comprises:

constructing a neural network for adjusting the formula for calculating the values of the set of parameters representing the overlay accuracy; and

comparing the values of the set of parameters representing the overlay accuracy with measured values for the set of parameters representing the overlay accuracy obtained in the inspection tool.

11. (original) The method according to claim 8, which comprises:

issuing a warning signal when one of the parameters of the set of parameters representing the overlay accuracy of the pattern increases beyond a predetermined tolerance level;

stopping processing with the exposure tool for conducting system maintenance in response to the warning signal; and

continuing with processing after resetting the exposure tool.

12. (original) The method according to claim 8, which comprises:

issuing a warning signal, when one of the parameters of the set of parameters representing the overlay accuracy of the pattern increases beyond a predetermined tolerance level; and

deriving the set of parameters representing the overlay accuracy of the pattern on the semiconductor wafer for a second time by measuring parameters with an overlay inspection tool after the semiconductor wafer has been exposed with the pattern.

13. (original) The method according to claim 8, which comprises processing each semiconductor wafer in a next

manufacturing step after being exposured without being inspected in an overlay inspection tool.

14. (original) The method according to claim 8, which comprises performing the step of adjusting the values of the second set of alignment parameters by calculating the values of the second set of alignment parameters from the values of the set of parameters representing the overlay accuracy using a formula that is a linear function having a respective coefficient for each of the alignment parameters of the second set of alignment parameters.